Experience in RF and Digital Design and Test

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superconducting electronics.

SUMMARY

- Experience in RFIC design and Testing RF modules
- RF Link Budget Analysis on millimeter wave SoC, MtM
- Experience with design, test, integration and manufacturing
- Digital design: Shifter, SRAM and Other CPU Blocks
- Familiarity with: JJ, SQUID, Quant_Entangl and RQL

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Outline

- RFIC Design and Testing of RF Modules in RF-Lab
- Digital Design: Successfully designed, tested and delivered different blocks of modern CPU
- Conducted Research on:
  - GaN (WBW) for Space Application
  - Novel Process beyond 10nm Nano Technology

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Contract @ Boeing Space

- Design Overview of Boeing Solid State Power Amplifier (SSPA) for Multiport Transceiver Systems for SLS.

- Design Overview of Solid State Power Amplifier (SSPA) and Multiport Transceiver Systems for Boeing Space. Proposed techniques to mitigate challenges such as Linearity, Gain, SSPA CLASSES, Power Consumption, AM-PM Conversion.

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Challenging Projects and how they were successfully delivered

- Main Challenging Project: RFIC and System Design for Space Application and Testing of RF modules
- Another Challenging Project: Successfully delivered Digital Design using Nano-Scale CMOS & SOI Technologies for leading edge Microprocessors

Note: There is NO company confidential or otherwise any propriety information on any of these slides

RFIC Design/Testing for Space Application

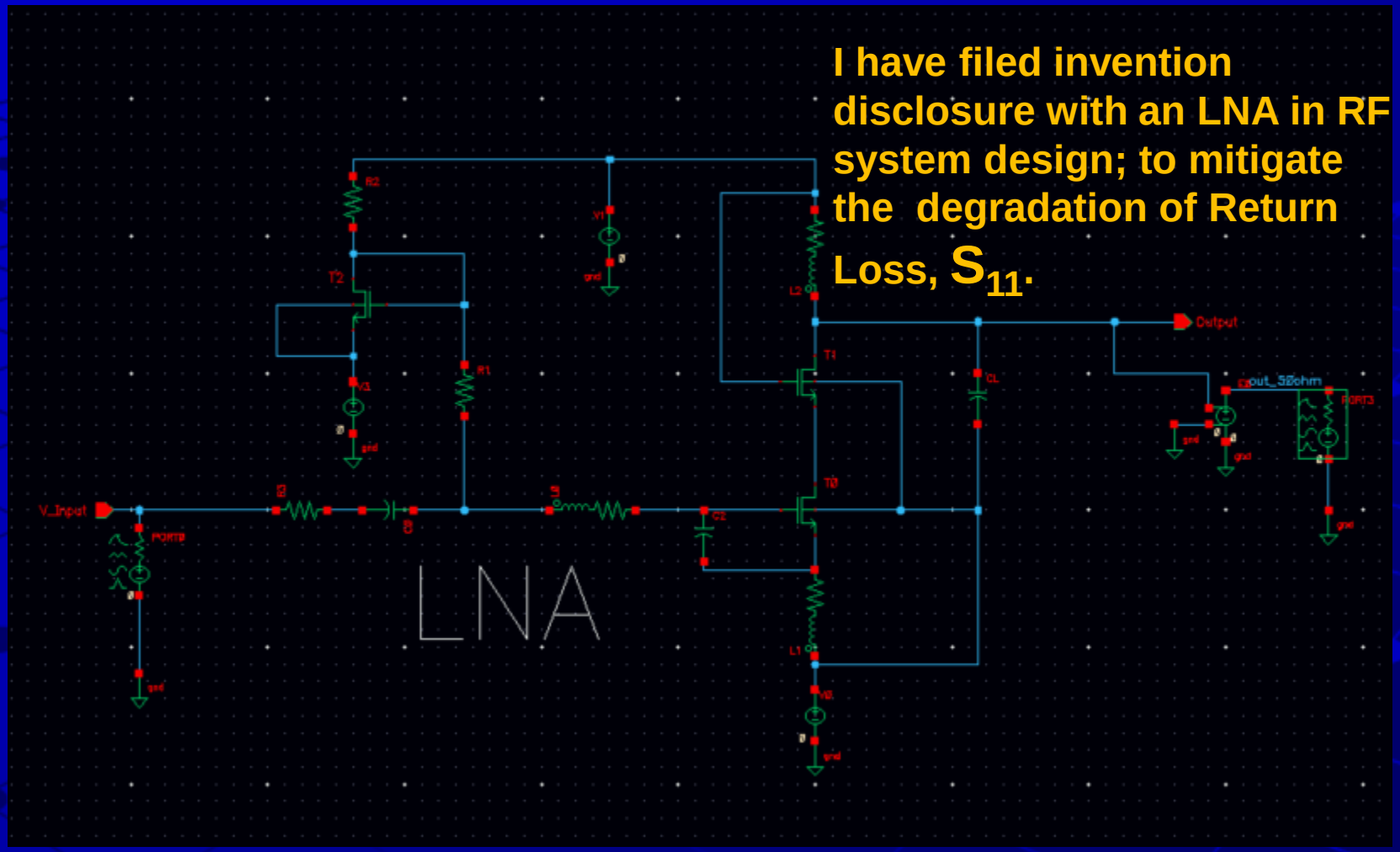
SITUATION/TASKS: No PDK was installed so using my EDA tool experience installed the PDK for RF design

ACTIONS: I had to learn two tools ADS (from Keysight) and RF-Spectra (from Cadence) rather quickly

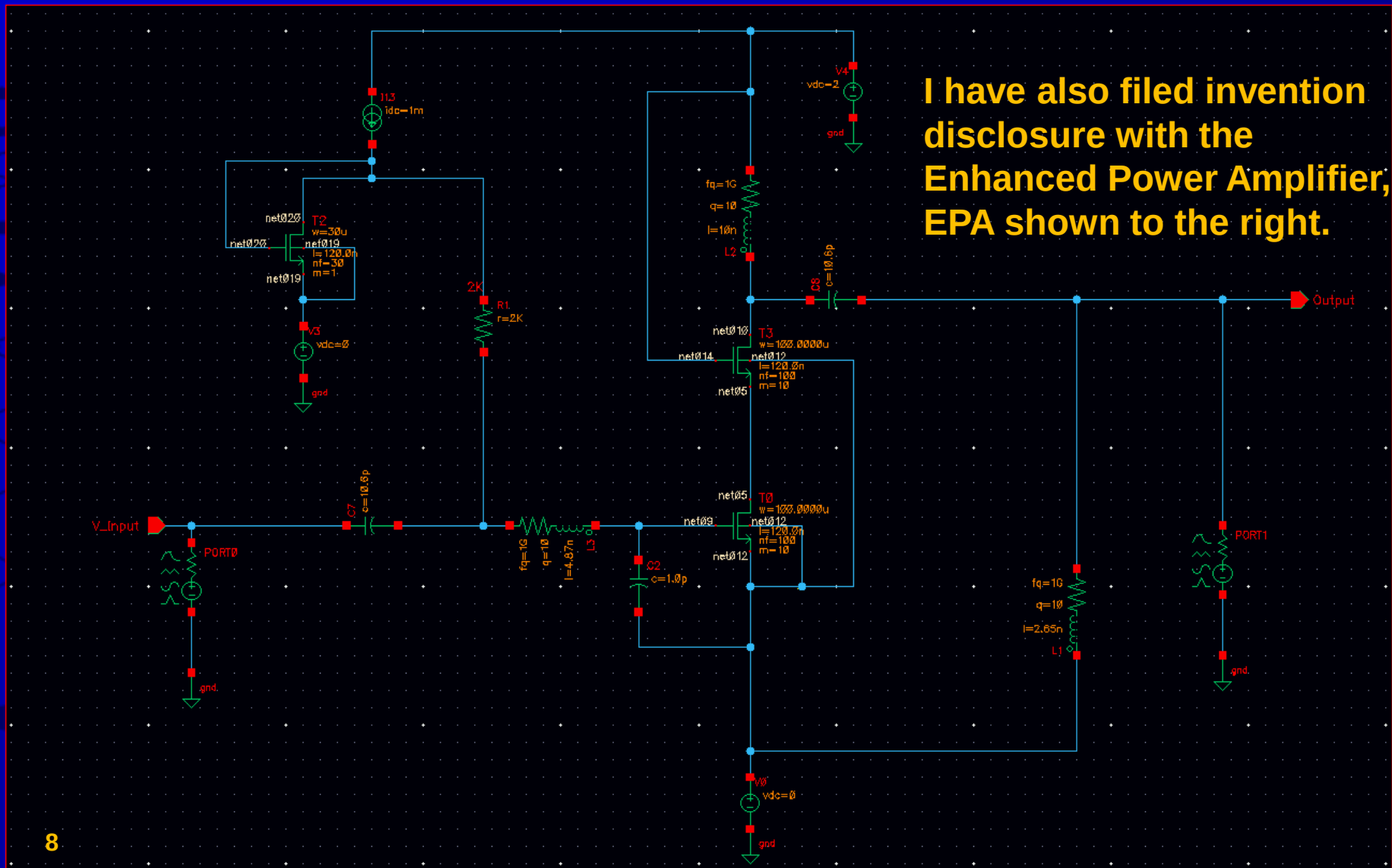
RESULTS:

Successfully Completed the RFIC Project: Designed LNA, PA (next page).

Circuit of Low Noise Amplifier



Cascaded PA: Better Stability, Higher Linearity & Lowering the miller effects



I have also filed invention disclosure with the Enhanced Power Amplifier, EPA shown to the right.

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Leadership Skills and Experience

- A) As a Lead engineer, trained and guided Electronic Engineers in the high tech at IBM, AMD and Northrop Grumman
- B) Coordinated and led RF Engineers for the RF Lab and wrote Test Procedures for the RF Team
- C) Experience with leading a team of engineers

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Robust and Reliable Design

- Solved complex technical issues on Design/Testing for Robustness on:
  - EM, IR drop and Noise
- Designed and tested both Digital and RF Modules with the Safety, Robustness and Longevity
- Mitigating the following issues for a Robust Design:
  - Noise, Electromigration, Low Power Supply
  - Electromagnetic Interference
  - Failures in a harsh environment

Challenging RF Lab Efforts: during the pandemic

- We followed the Lab procedure that two of us had written the previous day
- Then took the measurements and analyzed the data in the Lab

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- After some debugging efforts, went to the RF-Lab with better procedures
- RF System Design: Measured P1dB/IP3 for BB. Programmed Digital boards with LabView Software
- Coordinated manufacturing efforts at the lab
- I presented the Lab report to the management

IBM CPU Redesign from 130nm to 45nm CMOS SOI Technology.

SITUATION:

Challenges of Design in SOI Technology from CMOS

When a technology gets shrunk two things increase:

- 1. Variations and
- 2. Leakage Current

- Furthermore, it is almost impossible to achieve radiation hardness on modern process nodes

Redesigned IBM CPU from CMOS 130nm to 45nm SOI Technology

TASKS/ACTIONS:

- Leveraging my design, verification and Device Physics experience completed the complex design

- Gained precious experience in Silicon Debugging from the hardware failure analysis; this is a desired skill for a successful final product

RESULTS:

- Designed, Tested, Debugged and Successfully Delivered Microelectronics Chips to our customers

Summary of Low Power Design

Knobs for Low Power Design	CHANGE	Threshold V_{th}	Leakage Current, I_{Leak}
Device Length l	IF DECREASES	DECREASES	INCREASES
Device Width W	IF DECREASES	INCREASES	DECREASES
V_{BULK}	IF DECREASES	INCREASES	DECREASES
Doping-Cont N_A	IF INCREASES	INCREASES	DECREASES
Gate Thickn T_{Si}	IF DECREASES	DECREASES	INCREASES
Temperature	IF INCREASES	DECREASES	INCREASES

R&D: Motivation for Low Power Device beyond < 10nm Tech

The scaling of conventional Si-based MOSFETs is currently running into fundamental problems.

Hot electron effects, Velocity Saturation, Short Channel Effects, Punchthrough and Tunneling effects are some of challenging factors of CMOS Technology beyond 10nm gate length.

Hole Mobilities of Primary Semiconductors [$cm^2/V \cdot s$]

Si	Ge	AlGaAs	InGaAs	InP	GaN
450	1900	140 – 400	300 – 400	200	350

R&D: Next generation Nano-Scale novel Device

Alternate High-mobility channel materials is vital for the next generation of high-performance MOSFETs

Germanium (Ge) has been considered as an attractive channel material because of its higher carrier mobility and process compatibility with Si-based devices

Sentaurus Device Simulator was used. Output (I_D-V_{DS}) characteristics at various V_{GS} biases. Also, TCAD is used for Device Simulations. And Monte Carlo could be used

R&D Projects for GaN Technology

Research on RF-GaN Process for Space:

- **The main advantage of GaN is: It can have a Power Amplifier (PA) whose Drain Voltage can swing up to 40 volts**
- **The GaN device inherently poses the quality of Wide Band (WB) quality**

Software skills and experience

MATLAB:

- Simulated different complex equations and their graphs. GPS III Satellite project
- Goal was to determine the Gravity of the Moon

- Extensively worked in Unix (also in Linux) env

- Written Assembly, Scripting
- Courses taken at college: C++/C# and Python

Thank you!